

Appl. No. 09/828,041  
Response dated May 17, 2004  
Reply to Office Action of March 15, 2004

### **REMARKS/ARGUMENTS**

Claims 1-42 remain in the application. Of these, claims 12-28 and 33-42 stand allowed. Claims 7, 8, 10, 11, 31 and 32 stand objected to as being dependent on rejected claims, but are otherwise allowable. Claims 1-6, 9, 29 and 30 stand rejected.

#### **1. Rejection of Claims 1-6 & 9 Under 35 USC 102(b)**

Claims 1-6 and 9 stand rejected under 35 USC 102(b) as being anticipated by CD4018B CMOS counter, TI Data Sheet, 1998.

Applicants' claim 1 recites "counter control logic" that 1) enables a counter "before *each* strobe signal is received", and 2) resets the counter "after *each* strobe signal is received". The Examiner asserts that such counter control logic is described by CD4018B in FIGS. 15 & 17 (wherein FIG. 15 shows the use of a PRESET input to enable a counter). Applicants respectfully disagree.

Although the counter described by CD4018B may be enabled and reset, CD4018B does not teach that enablement and reset of the counter are in any way tied to the counter's receipt of *each* of a number of strobe signals. Rather, it seems that the counter described by CD4018B merely updates a count in response to a *single, continuous clock signal*. In other words, although CD4018B's counter may be enabled and reset as desired, enablement and reset of the counter have no relation to starts, stops or changes in the clock signal received by the counter.

Applicants' claim 1 further recites that its "counter control logic" resets its counter "after each strobe signal is received by receiving feedback from said counter". The Examiner asserts that such a reset is shown by CD4018B in FIG. 17, but applicants disagree. CD4018B's FIG. 17 shows counter feedback being provided to an IC's data (D) input. However, the IC's reset (R) input is grounded, and therefore does not receive counter feedback, as the Examiner suggests.

Applicants' claim 1 is therefore believed to be allowable over the teachings of CD4018B in that CD4018B does not teach nor suggest counter control logic that

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enables and resets a counter as recited in applicants' claim 1. Claims 2-4 are believed to be allowable over CD4018B at least for the reason that they depend from an allowable claim 1.

Applicants' claim 5 is believed to be allowable over CD4018B for reasons similar to those that make claim 1 allowable over CD4018B. That is, CD4018B does not teach nor suggest "counter control logic" that 1) enables a counter "before *each* strobe signal is received", and 2) resets the counter "after *each* strobe signal is received by i) receiving feedback from said counter".

Claims 6 and 9 are believed to be allowable over CD4018B at least for the reason that they depend from an allowable claim 5. Claim 6 is also believed to be allowable in that CD4018B does not specify that its counter is a rollover counter. Claim 9 is also believed to be allowable in that CD4018B does not disclose "start and stop conditions [being] generated on a single signal line". Rather, CD4018B only discloses an IC with separate RESET and PRESET inputs, with no connection therebetween.

## 2. Rejection of Claims 1-6 & 9 Under 35 USC 102(a)

Claims 1-6 and 9 stand rejected under 35 USC 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

Applicants' claim 1 recites "counter control logic" that 1) enables a counter "before *each* strobe signal is received", and 2) resets the counter "after *each* strobe signal is received". The Examiner asserts that such counter control logic is described by Manning in col. 2, lines 40-42. Applicants respectfully disagree.

As taught by Manning,

...the Counter 50 is an 8 stage quadrature counter which decrements from 255 to 0 responsive to the clock signals, CLK and clock CLK 90.

Manning, col. 5, lines 6-9.

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Manning also teaches that CLK and CLK 90 are "generated by a conventional clock circuit 28" (col. 4, lines 11-13).

In light of Manning's above teachings, it is Applicants' position that Manning's counter is not enabled and disabled before/after receipt of each of a number of strobe signals. Rather, it seems that Manning's counter 50 receives a pair of continuously generated clock signals, but only decrements (i.e., counts) in response to the clock signals during periods when it is enabled to do so.

Applicants' claim 1 further recites that "counter control logic" resets a counter after each strobe signal is received by "receiving feedback from said counter". The Examiner asserts that such a reset based on counter "feedback" is taught by Manning in col. 5, lines 62-65. Applicants respectfully disagree.

As taught by Manning,

... At or before the terminal count, other circuitry in the integrated circuit causes the STOP signal to go active high, thereby causing the Counter Control circuit 46 to disable the Counter 50.

Manning, col. 5, lines 62-65.

Applicants believe it is too great a jump to conclude that the above statement supports resetting a counter based on feedback from the counter. Although Manning states that a STOP signal is caused to go active high "at or before the terminal count", Manning also states that it is "other circuitry in the integrated circuit" that causes the STOP signal to go active high. Manning does not state that the terminal count of the counter 50 is fed back to the "other circuitry". In fact, Manning says very little about how the "other circuitry" operates. Applicants therefore believe the Examiner is improperly using hindsight and their own teachings to read more into Manning than what Manning actually teaches.

For the above reasons, applicants' claim 1 is believed to be allowable over the teachings of Manning. Claims 2-4 are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 1.

Applicants' claim 5 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning. That is, Manning does not teach nor suggest "counter control logic" that 1) enables a counter "before *each* strobe

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signal is received", and 2) resets the counter "after each strobe signal is received".  
Claims 6 and 9 are believed to be allowable over Manning at least for the reason that they depend from an allowable claim 5.

### 3. Rejection of Claims 29 & 30 Under 35 USC 102(a)

Claims 29 and 30 stand rejected under 35 USC 102(a) as being anticipated by Manning (U.S. Pat. No. 6,230,245).

Applicants' claim 29 is believed to be allowable over Manning for reasons similar to those that make claim 1 allowable over Manning. Claim 30 is believed to be allowable over Manning at least for the reason that they depend from an allowable claim 29.

### 4. Conclusion

Given the above Remarks, applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,  
DAHL & OSTERLOTH, L.L.P.

By: 

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